

BOLBO = IEEE CMP/IP Support Repository Component

ECE715/992 Project

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- **BOLBO**

Background

The project has several purposes:

1. A course project for *ECE715. Introduction to VLSI*
2. A library component for the IEEE CMP/IP Support Repository
3. A SoC application with enhanced BIST capability
4. A pilot for the repository development
5. A comparison framework for different modeling languages:
 - ASIC/VLSI using scaleable MOSIS technology;
 - VHDL description at different levels: behavioral; RTL, and gate levels
 - Simulink description

Design Specs

Design a $(1024 + r)$ -bit shift-register to be used as BOLBO (Build-Out-Logic-Block-Observer) circuits. The shift-register will be partitionable to the 8-bit-level. The individual partitions will be provided with their respective modulo-two feedback polynomials for test purposes. All shift-register bits will be accessible at the chip level. The shift-register content, the partition markers and the polynomial selection markers will be entered sequentially through a JTAG port. The shift-register will be fault-tolerant, individual bits can be bypassed. Lastly, a reasonable value of r will be determined as a function of expected process and product yields. The shift-register content and the valid-bit markers will be read out through a JTAG port. Select the appropriate package. Provide a concept-of-operation user manual and test plan.

Block Diagram & Pin Assignment

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Reading Materials

- DFT
- Signature Analysis
- LFSR
- Pseudo random test generator
- BIST
- systemBIST

- JTAG
- BILBO

Design Methodology

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Concept-of-Operation User Manual

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Test Plan

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- BOLBO Compliant SoC

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References

- [CJC03] CJ Clark and Mike Ricchetti, "Infrastructure IP for Configuration and Test of Boards and Systems", *IEEE Design & Test of Computers*, May-June 2003
- [BLE93] H. Bleeker et al., *Boundary Scan Test: A Practical Approach*, Kluwer Academic Publishers, Dordrecht, 1993
- [PER07] Evgeni Perelroyzen, *Digital Integrated Circuits DFT Using Simulink and StateFlow*, CRC Press. 2007
<http://www.ee.ncu.edu.tw/~ccsu/Teach/Test/HandOuts/BIST.doc>
http://www.imit.kth.se/courses/2B1423/0405/F8_6.pdf